THE AFFECT OF THERMAL PERFORMANCE ON DEVICE CURRENT UTILISATION

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Abstract - A *significant improvement in power-semiconductor-device utilisation seems possible if the maximum output current of power-stages could be limited by thermal feedback from the power-converter. To illustrate the potential utilisation benefit obtained in main switching devices, the variation in usable current with operating conditions is examined for several devices applied in a constant-frequency-PWM VVVF inverter, and operated under conditions to keep their junction-temperature constant.*

INTRODUCTION

Typical errors that exists in heatsink design calculations are often not precisely known or empirically tested despite the strong influence power-device junction temperature has on failure-rate, and thus power electronics system reliability, and the contribution of the heatsink assembly to overall system size and weight. The likely reasons for this include: the difficulty in accurately predicting or even bracketing device power-loss, given the existence of production-spread and temperature variation in conduction and switching characteristics; the complexity of practical power-loss waveforms; the imprecision in estimated thermal impedance and resistance seen by power devices distributed on a heatsink; and the difficulty in measuring the chip-area-averaged junction-temperature of switched power-devices. As a result of such difficulties, the safety margins built into power-stage and heatsink designs will often be far from optimum.

Some improvement in verifying the operating junction-temperature of devices and achieving tighter designs will inevitably result from better loss prediction and thermal-design verification as simulation tools become more widely tested and developed. However, a greater improvement in optimizing device utilisation, and incidentally system reliability, seems possible from more sophisticated active current-limiting, which limits the maximum output current or power of systems to maintain the junction-temperature (or power dissipation) of the main power-devices below a pre-set level, say 125 °C, on a pulse-by-pulse basis. The effects of changes in device heating and cooling characteristics due to dynamic load changes, variation in operating conditions etc. would, thus, be directly measured and safeguarded against, by closed-loop control.

There would be significant practical difficulties to overcome in implementing temperature-regulated active-current-limiting, such as obtaining clean, proportional, die-area-averaged, junction-temperature feedback signals, or on-line monitoring of converter input and output power, without adding significantly to device cost. But prior to tackling these, it is necessary to clearly establish the incentive for developing such a control scheme by considering the potential level of increase in device utilisation. This has been investigated, in principle, by notionally applying a range of medium-power devices in a constant-frequency PWM three-phase inverter application and estimating the maximum usable current that gives a specific junction temperature for a range of varying modulating and switching frequencies.

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ESTIMATING DEVICE POWER-LOSS IN INVERTERS

Examining device efficiency and current utilisation level in a PWM inverter, rather than the more common test set-up of a single-ended chopper, involves greater analytical complexity because device current and duty-cycle vary sinusoidally, and the variation in all loss components with current level must be determined and averaged over an output-frequency, f_O, period. The averaging, however, becomes relatively simple with high carrier-frequency ratio, p, [i.e. p or $f_{SW}/f_O \geq 10$], provided conduction power-loss and switching energy-loss equations can be expressed as continuous functions of current, because discrete-equation averages may then be approximated by closed-form continuous-equation averages.

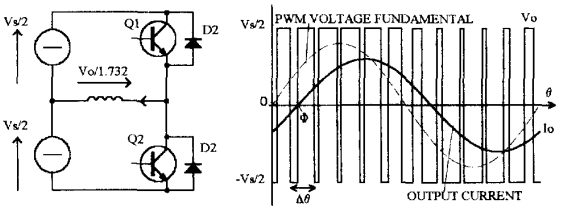

Fig.1 Equivalent circuit for power-loss estimation; and PWM voltage, its fundamental component, and lagging output current.

The power-loss in each of the bridge-legs of a 3-phase inverter is the same, assuming steady-state machine operation, and it is only necessary to examine the equivalent circuit for one bridge-leg and load-phase shown in Fig.1. Also, the inductive load, i.e. the machine-winding, is assumed to draw a pure sinusoidal current since the inverter switching period is usually chosen to be far less than the winding time-constant to give low current-ripple.

The calculation of average bridge-leg power-loss in asynchronous regular-sampled-PWM inverters has been the subject of previous investigations [5-11]. Generally, these either involve the numerical solution of discrete loss equations [5,11], or the use of approximate closed-form solutions to discrete equations [6-10]. The latter method of solution, although inherently less flexible and accurate, avoids the need to generate such complex algorithms for numerical solution by computer, and has been shown [9] to give surprisingly low error for regular-sampled-PWM, provided p is at least 10.

CONDUCTION POWER-LOSS

Switch and diode on-state characteristics are approximated here using conventional piece-wise linear models [Eqs.(1a) and (1b)] but may be specified as a more precise function of current using simulated or measured device on-state characteristics, if greater accuracy is desired.

$$v_Q(i) = V_{QO} + i\,r_Q \qquad (1a)$$

$$v_D(i) = V_{DO} + i\,r_D \qquad (1b)$$

Bridge-leg current at any instant, θ, of the fundamental output-period is given by Eq.(2), where $\theta = \omega t$ and ϕ is the phase difference between the load-current and PWM voltage-waveform fundamental [see Fig.2].

$$i(\theta) = \hat{I}_O \sin(\theta - \phi) \tag{2}$$

Transistor and diode normalised conduction periods at any θ are given by Eqs.(3a) and (3b), where M is the modulation index and $\Delta\theta$ is $2\pi/p$.

$$\Delta\theta_Q = \frac{1}{2}[1 + M\sin\theta]\Delta\theta \tag{3a}$$

$$\Delta\theta_D = \frac{1}{2}[1 - M\sin\theta]\Delta\theta \tag{3b}$$

Therefore, net average conduction power-loss over 2π is given by Eqs.(4a) and (4b).

$$P_{QCON} = \frac{1}{2\pi}\sum_{s=\phi/\Delta\theta}^{(\pi+\phi)/\Delta\theta}\left[V_{QO}\, i(s\Delta\theta) + r_Q i^2(s\Delta\theta)\right]\Delta\theta_Q \tag{4a}$$

$$P_{DCON} = \frac{1}{2\pi}\sum_{s=\phi/\Delta\theta}^{(\pi+\phi)/\Delta\theta}\left[V_{DO}\, i(s\Delta\theta) + r_D i^2(s\Delta\theta)\right]\Delta\theta_D \tag{4b}$$

Approximate closed-form solutions are obtained by assuming $\Delta\theta$ tends to zero and using continuous system averages given by Eqs.(5a) and (5b).

$$P_{QCON} \approx \frac{1}{2\pi}\int_{\phi}^{\pi+\phi}\left[V_{QO} i(\theta) + r_Q i(\theta)^2\right]\frac{[1 + M\sin\theta]}{2}\, d\theta \tag{5a}$$

$$P_{DCON} \approx \frac{1}{2\pi}\int_{\phi}^{\pi+\phi}\left[V_{DO} i(\theta) + r_D i(\theta)^2\right]\frac{[1 - M\sin\theta]}{2}\, d\theta \tag{5b}$$

These, when solved, give the following diode and switch average conduction power-loss equations.

$$P_{QCON} \approx \frac{\hat{I}_O V_{QO}}{2}\left(\frac{1}{\pi} + \frac{M}{4}\cos\phi\right) + \hat{I}_O{}^2 r_Q\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right) \tag{6a}$$

$$P_{DCON} \approx \frac{\hat{I}_O V_{DO}}{2}\left(\frac{1}{\pi} - \frac{M}{4}\cos\phi\right) + \hat{I}_O{}^2 r_D\left(\frac{1}{8} - \frac{M}{3\pi}\cos\phi\right) \tag{6b}$$

Although these loss equations do not incorporate the effects of third-harmonic addition, which is later assumed to be used, the difference in loss may be shown to be small.

SWITCHING POWER-LOSS

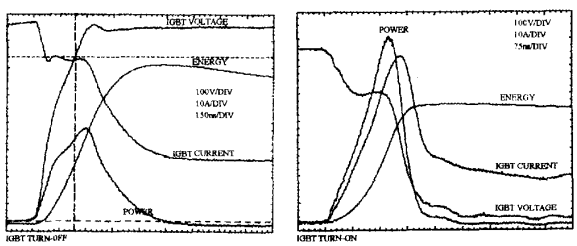

Fig.2 Switching waveforms and extracted power and energy graphs

Switching loss comprises turn-on and turn-off loss components arising from crossover in device current and voltage waveforms. The heat energy added at each switching interval is now readily measurable with high-bandwidth digital oscilloscopes, which perform waveform multiplication and integration to give instantaneous power and energy change [see Fig.2], and increasingly graphs of switching energy versus current are being supplied by device manufacturers. Wherever possible, such direct loss measurements are used. For those devices for which loss data is unavailable, switching energy is estimated from switching time data.

Turn-off switching energy

Power-device switching performance is often estimated from turn-off current fall, t_{FI}. However, experimental and published switching waveforms generally show that 50% or more of the turn-off loss occurs during the voltage rise with high-voltage devices. Therefore, if switching crossover time measurements, $t_{C(off)}$, are unavailable, Eq.(7b), rather than Eq.(7a), is used for loss estimation. The 0.8 factor arises due to measurement at 10 or 90% levels.

$$W_{QSW(off)}(\theta) = \frac{1}{2}V_S I(\theta)\frac{t_{C(OFF)}}{0.8} \tag{7a}$$

$$W_{QSW(off)}(\theta) = V_S I(\theta)\frac{t_{FI}}{0.8} \tag{7b}$$

Where switching energy-loss measurements do exist, the relationship between $W_{QSW(off)}$ and switched current at any instant may be approximated by Eq.(8) in many cases, where W_{QR} is the turn-off energy-loss at a reference current value I_{QR} and n is the gradient of the loss graph when plotted on logarithmic axes.

$$W_{QSW(off)}(\theta) = \left(\frac{I(\theta)}{I_{QR}}\right)^n W_{QR} \tag{8}$$

Loss graphs for many of the devices considered later are plotted from published data in Fig.3. Appendix-1, Table-2 gives further device details.

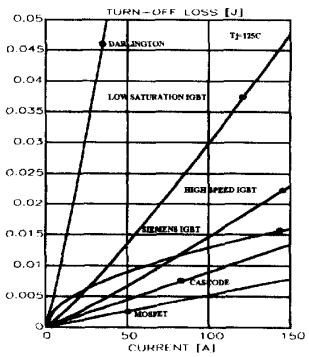

Fig.3 (a) Approximate turn-off energy-loss versus switched-current graphs for various devices after parabolic curve fit

With sinusoidally modulated current $W_{QSW(off)}$ at any switching instant is given by Eq.(9), and Eq.(10) gives the total average power-loss. The remaining integration in Eq.(10) cannot be solved explicitly and must be approximated by numerical solution.

$$W_{QSW(off)}(\theta) = \left(\frac{\hat{I}_O}{I_{QR}}\sin\theta\right)^n W_{QR} \tag{9}$$

$$P_{QSW(off)}(\theta) = \frac{f_{SW}}{2\pi}\left(\frac{\hat{I}_O}{I_{QR}}\sin\theta\right)^n W_{QR}\int_0^{\pi}\sin^n\theta\, d\theta \tag{10}$$

The evaluation of average power-loss relies on specifying switching energy-loss as a continuous function of current which is then easily integrated. It should be noted that the derived loss equations, such as Eqs.(8) to (10), are merely examples, and their form, as well as their coefficients, may be adjusted for greater accuracy or new devices.

Turn-on switching energy

The variation in turn-on energy-loss with current, $W_{QSW(on)}$ may also be approximated by Eq.(8). Where directly measured $W_{QSW(on)}$ data is unavailable, $W_{QSW(on)}$ may be estimated using diode reverse-recovery charge, Q_{RR}, data.

With a stiff drive circuit and little series parasitic-inductance, switch turn-on waveforms, with current freewheeling in a fast-recovery diode, are similar to those in Fig.2, where Q_{RR} is assumed to be fully discharged while the switch voltage, v_Q, is high at approximately, V_S. $W_{QSW(on)}(\theta)$ may then be estimated from Eq.(11).

$$W_{QSW(on)}(\theta) = \int_0^{t_{RI}+t_S} v_Q i_Q dt = V_S\left(Q_{RR} + I(\theta)\sqrt{\frac{2Q_{RR}}{di/dt}} + \frac{I(\theta)^2}{2di/dt}\right) \tag{11}$$

With modulated current $W_{QSW(on)}(\theta)$ must be averaged over an output frequency period. Recovery di/dt is assumed sufficiently high (>400 A/μs), such that Q_{RR} approaches the total stored charge in the diode, and is approximately proportional to forward current. Q_{RR} is then given at any current by Eq.(12a), where Q_{RRR} is the recovered charge at a reference current I_{DR}, and, for sine-weighted PWM, Eq.(12b) gives Q_{RR} at each switching instant, θ.

$$Q_{RR}(\theta) = \frac{I(\theta)}{I_{DR}} Q_{RRR} \tag{12a}$$

$$Q_{RR}(\theta) = \frac{\hat{I}_O}{I_{DR}} Q_{RRR} \sin\theta \tag{12b}$$

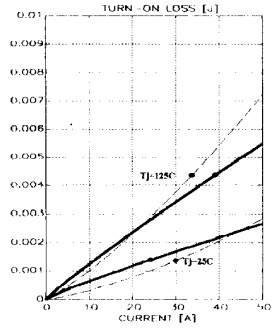

Fig.3 Measured turn-on energy-loss (cont.) for BSM50GB100D with loss estimated from Q_{RR} (dash) with correction for stray-inductance associated volt-drop

A turn-on power-loss graph derived using Eq.(11) with a single Q_{RR} measurement, is overlaid on a curve fit to manufacturer's $W_{QSW(on)}$ data in Fig.3. Compensating for stray inductance in the energy-loss calculation is necessary and allows the error to be reduced to ≈30%. With sinusoidal load-current, $P_{QSW(on)}$ at any switching instant is given by Eq.(13), which gives Eq.(14) when averaged over 2π.

$$P_{QSW(on)}(\theta) = f_{SW}V_S\left(\frac{\hat{I}_O}{I_{DR}} Q_{RRR}\sin\theta + \hat{I}_O \sin^{\frac{1}{2}}\theta\sqrt{\frac{2\hat{I}_O / I_{DR}}{di/dt}} + \frac{\hat{I}_O^{\,2}}{2di/dt}\sin\theta\right) \tag{13}$$

$$P_{QSW(on)} \approx \frac{f_{SW}V_S}{2\pi}\left(2\frac{\hat{I}_O}{I_{DR}} Q_{RRR} + 2.472\hat{I}_O\sqrt{\frac{Q_{RRR}\hat{I}_O / I_{DR}}{di/dt}} + \frac{\pi\hat{I}_O^{\,2}}{4di/dt}\right) \tag{14}$$

When a graph of $W_{QSW(on)}$ measurements is available, and a parabolic-curve approximation to it using Eq.(15) is possible, $P_{QSW(on)}$ is obtained by averaging Eq.(15) over 2π to give Eq.(16), as previously performed for $P_{QSW(off)}$.

$$W_{QSW(on)}(\theta) = \left(\frac{\hat{I}_O}{I_{DR}}\sin\theta\right)^m W_{DR} \tag{15}$$

$$P_{QSW(on)} \approx \frac{f_{SW}V_S}{2\pi}\left(\frac{\hat{I}_O}{I_{DR}}\right)^m W_{DR}\int_0^{\pi}\sin^m\theta\, d\theta \tag{16}$$

Total power-loss

The total conduction and switching loss produced by a bridge-leg switch-diode pair, P_{QD}, may now be calculated by collecting power-loss terms as shown in Eq.(17). Note, that diode switching loss is assumed negligible, at this point,. Where parabolic switching-loss equations are appropriate, P_Q and P_D are given by Eqs.(18a) and (18b).

$$P_{QD} = P_Q + P_D = \left(P_{QCON} + P_{QSW(on)} + P_{QSW(off)}\right) + P_{DCON} \tag{17}$$

$$P_{Q\Sigma} \approx \frac{\hat{I}_O V_{Q0}}{2}\left(\frac{1}{\pi} + \frac{M}{4}\cos\phi\right) + \hat{I}_o^{\,2} r_Q\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right) + \frac{f_{SW}}{2\pi}\left\{\left(\frac{\hat{I}_o}{I_{QR}}\right)^n W_{QR}\int_0^{\pi}\sin^n\theta\, d\theta + \left(\frac{\hat{I}_O}{I_{DR}}\right)^m W_{DR}\int_0^{\pi}\sin^m\theta\, d\theta\right\} \tag{18a}$$

$$P_{D\Sigma} \approx \frac{\hat{I}_O V_{D0}}{2}\left(\frac{1}{\pi} - \frac{M}{4}\cos\phi\right) + \hat{I}_o^{\,2} r_D\left(\frac{1}{8} - \frac{M}{3\pi}\cos\phi\right) \tag{18b}$$

Net inverter power-stage efficiency, η_{INV} is then given by Eq.(19), where S_O is inverter apparent output power.

$$\eta_{INV} \approx \frac{S_O\cos\phi}{S_O\cos\phi + 6P_{QD}} \tag{19}$$

DERATING POWER DEVICES

Power devices must be operated below their absolute maximum ratings in most applications for an acceptable service life [21, 22]. Current, voltage and power, or junction-temperature, derating must also be performed to allow for production spread in device characteristics, tolerance in design calculations, line-voltage surges, and cost effective heatsink design.

Current derating

The most significant current derating arises from the impracticality of maintaining device case temperature, T_C, at 25°C, i.e. the case temperature for which rated device-current is often specified, hereafter termed T_{CS}. Power devices are normally operated with $T_{C(max)}$ at 70-80°C at maximum ambient temperature to keep heatsink requirements practical while allowing reasonable device utilisation. For case temperatures above 25°C, power-loss must be linearly derated from the maximum allowable value at T_{CS}, P_{QS}, according to Eq.(24), to keep junction temperature, T_j, at or below $T_{J(max)}$, which is usually 150°C.

$$P_Q(T_C) = \left(\frac{T_J - T_C}{T_{J(MAX)} - T_{CS}}\right) P_Q(T_{CS}) \tag{24}$$

A stress-ratio derating is then indirectly applied by reducing operating T_J below 150°C to give reasonable equipment service life. A value of T_J=110°C will be used here as the maximum working junction temperature, $T_{J(wmx)}$, based on recommendations for non hermetically sealed packages [21].

TRANSIENT THERMAL IMPEDANCE CONSIDERATIONS

From the maximum permissible average device power-loss at $T_{J(wmx)}$, P_Q ($T_{J(wmx)}$), the maximum permissible switch current is readily obtained for rectangular current pulses of width t_P and duty-cycle ratio D from Eq.(25) by solving for $\hat{I}_O$.

$$\frac{P_Q(\hat{I}_O)}{D} = \frac{(T_{J(wmx)} - T_{C(max)})}{Z(t_P, D)R_{\theta JC}} \tag{25}$$

Modifying Eq.(25) to include diode loss and device-case-to-heatsink thermal resistance, $R_{\theta CH}$, across which 5-10°C may be dropped, thus rendering it usable with bridge-leg modules, gives Eq.(26). This is, henceforth, used to determine maximum $\hat{I}_O$ by assuming heatsink surface, T_H, rather than case, T_C, temperature is limited to 70°C.

$$\frac{P_Q(\hat{I}_O)}{D} = \frac{T_{J(wmx)} - \left\{\left[P_Q(\hat{I}_O) + P_D(\hat{I}_O)\right]R_{\theta CH} + T_{H(max)}\right\}}{Z(t_P, D)R_{\theta JC}} \tag{26}$$

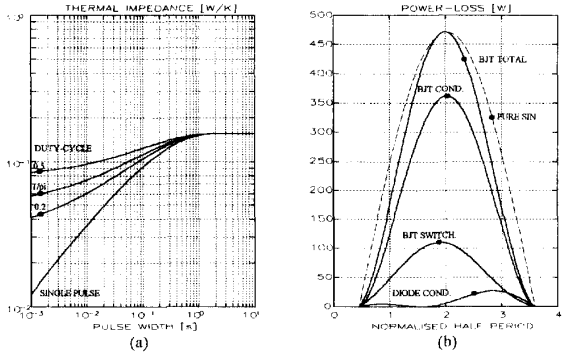

Fig.4 Darlington BJT, MG150M2YK1 (a) single-pulse and repetitive transient thermal-impedance characteristics and (b) quasi-instantaneous conduction and switching power-loss components for f_{SW}=5kHz, f_O=50Hz and T_J=110°C

In sine-weighted PWM inverters, device quasi-instantaneous power pulses, obtained by averaging instantaneous power-loss over each f_{SW} switching period, approximate to sine pulses as shown in Figs.4 and 5, and an equivalent rectangular power-pulse with the same amplitude and area may be used to give a conservative estimate of heating effect [23, 24]. Solving for $\hat{I}_O$ that gives T_J=110°C or any other T_J for given f_{SW} and f_Q values, therefore, proceeds by putting total average transistor and diode loss, P_Q and P_D, expressed in terms of $\hat{I}_O$, in Eq.(26), and then solving for $\hat{I}_O$, assuming P_Q originates in a rectangular pulse of amplitude πP_Q and width and duty-cycle $t_P = 1/\pi f_O$ and $D = 1/\pi$, since a rectangular pulse of such dimensions produces the same heating effect as a sine pulse of width $1/2f_O$, duty-cycle $1/\pi$, and amplitude πP_Q.

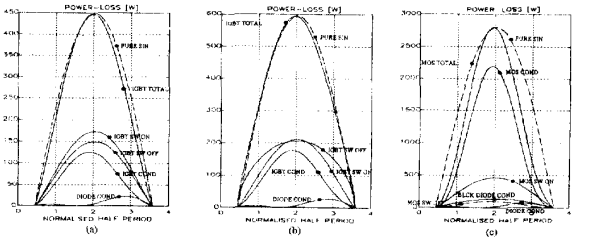

Fig5 (a) High-speed IGBT, MG150Q2YS1, (b) IGBT, BSM150GB100D and (c) MOSFET, BSM191C quasi-instantaneous conduction and switching power-loss components for f_{SW}=20kHz, f_O=50Hz and T_J=110°C operation at peak output current.

EVALUATION OF USABLE DEVICE CURRENT

The evaluation of usable current is most simply determined by calculating device loss and T_J for each f_{SW} or f_O value over a range of operating conditions as inverter I_O is increased, as shown in Fig.6. and collecting all the $\hat{I}_{O(max)}$ values giving the required $T_{J(wmx)}$.

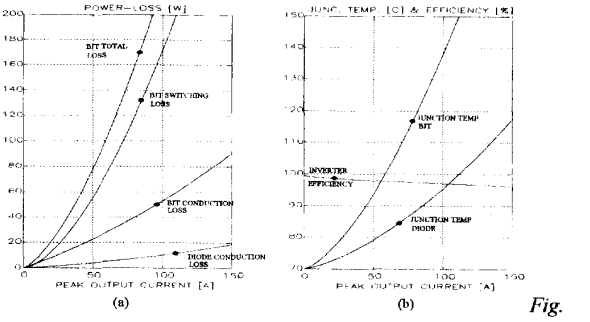

Fig. 6 Darlington MG150M2YK1 (a) bridge-leg transistor and diode power-loss components and (b) junction temperature and inverter efficiency versus peak inverter output current

This is exemplified for the Darlington BJT module in Fig.7 where $\hat{I}_{O(max)}$ variation with f_o and f_{SW} are given. The corresponding net inverter efficiency values may be similarly collected and plotted.

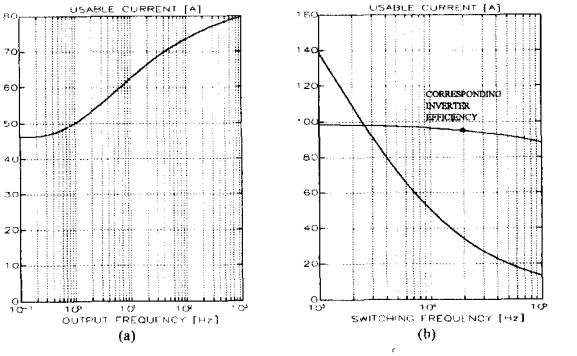

Fig.7 Darlington BJT, MG150M2YK1 maximum peak usable inverter output current $I_{M(max)}$ versus (a) inverter output frequency f_O with f_{SW}=5kHz and (b) inverter switching frequency f_{SW} with f_O=50Hz for $T_J \leq 110$°C

The increase in $\hat{I}_{O(max)}$ with f_O, seen in Fig.7a, results from the improved filtering effect of package thermal inertia and reduced T_J ripple. Usable $\hat{I}_{O(max)}$ is at least 50% higher at f_O =50Hz than f_O=0.5Hz, making adaptable current limiting of considerable benefit in VVVF applications to enable full device utilisation.

The rapid decrease in $\hat{I}_{O(max)}$ with f_{SW}, seen in Fig 7b, results from increasing switching-loss. A simple relationship between $\hat{I}_{O(max)}$ and f_{SW} is not specifiable, even though switching loss varies proportionally with frequency, because conduction and switching loss vary faster than proportionately with current. Hence $\hat{I}_{O(max)}$ decreases more slowly than in inverse proportion to f_{SW}.

From Fig.7 it is seen that, for operation at f_{SW}=5kHz and f_O=50Hz, $\hat{I}_{O(max)}$ is limited to 71A for the Darlington BJT. This is confirmed by practical experience because the device is recommended for and applied in 33kVA, 415V AC inverters [13, 15] with a maximum continuous r.m.s. output-current capability of 49.5A [i.e. with 110% continuous current overload because the nominal rated output is 45A r.m.s.], which corresponds to an $\hat{I}_{O(max)}$ of 70A.

Making allowance for production spread in device characteristics necessitates further current derating if typical data sheet on-state voltage and switching loss coefficient values are initially used. Maximum on-state voltage and switching parameters are often specified and were used, whenever available, in determining the presented device usable current values.

Generally, typical 125°C conduction and switching loss data is used without scaling for device utilisation prediction and comparison at 110°C. Similarly, 125°C freewheel-diode conduction and reverse-recovery data is used to considerably simplify the determination of $\hat{I}_{O(max)}$ in bridge-leg modules. Precise determination of freewheel-diode T_J is usually prevented by the absence of any data to calculate the switching-loss associated with diode current-fall and voltage-rise. Estimation of diode T_J [see Fig.6b] will therefore be low.

Usable switch current is not only dependent on switching and conduction loss, but, also, on allowable T_J stress-factor, device package and heatsink thermal performance, production tolerance in characteristics, and freewheel-diode reverse-recovery performance. The switch-current derating calculation, therefore, cannot be reduced to a simple multiplication by a stress-factor, but is obtained from a more complex calculation, the aim of which is to find the $\hat{I}_{O(max)}$ corresponding to the power-loss giving the derated maximum junction temperature. By operating at or below $\hat{I}_{O(max)}$, it is unlikely that any of the absolute maximum peak, average or r.m.s. device currents will exceed the manufacturer recommended derated values; but this should be confirmed.

VARIATION IN DEVICE UTILISATION

Maximum usable peak inverter current, $\hat{I}_{O(max)}$, is evaluated for a range of 1000-1200V, 150A device technologies, when operated with T_J at 110°C in a 415V AC off-line inverter. Power loss graphs are given in Fig.8 for the devices when operated in an inverter at the same, $\hat{I}_O$, and illustrates differences in the levels of conduction and switching power-loss and their temperature sensitivity.

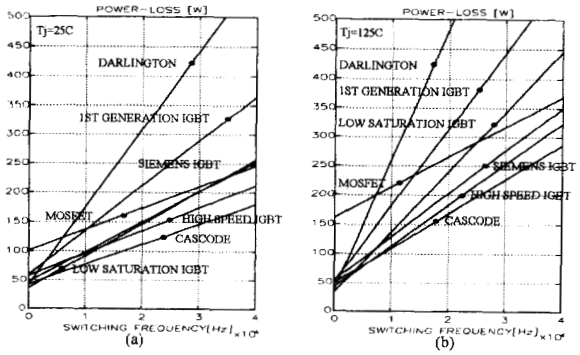

Fig.8 Total half bridge-leg conduction and switching loss versus f_{SW} for several 1000V, 150A devices when operated at 20kHz

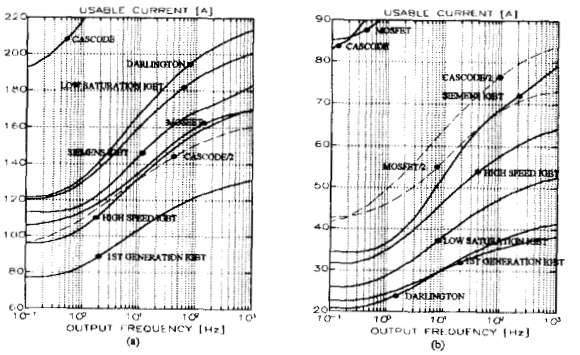

Fig.9 Peak usable half-sinewave current $\hat{I}_O$ versus inverter output frequency f_O for devices with T_J=110°C and f_{SW}=20kHz (a) if only conduction loss existed (b) with conduction and switching loss

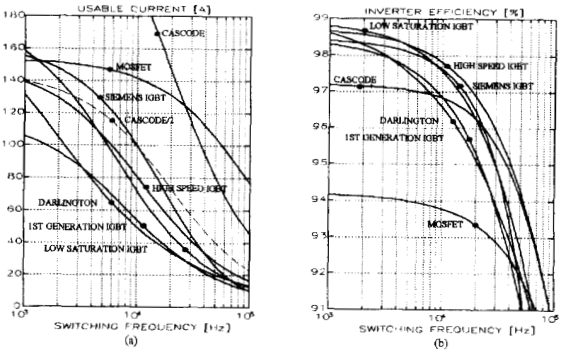

Fig.10 (a) Peak usable half-sinewave current $\hat{I}_O$ versus switching frequency f_{SW} for devices with T_J=110°C and with f_O=50Hz (b) corresponding inverter efficiency η_{INV} versus f_{SW}

Usable current of switches at high frequency

The variation in usable $\hat{I}_{O(max)}$ and inverter power-stage efficiency, η_{INV}, with f_O and f_{SW} is shown in Figs.9 and 10, and spot values for operation at f_O=50Hz, f_{SW}=20kHz and T_J=110°C are given in Table-1. The low $R_{\theta JC}$ of the cascode-switch, 150A, single-BJT, compression-capsule package allows its use at about twice the $\hat{I}_{O(max)}$ of all other devices except the MOSFET switch, irrespective

of f_O and f_{SW}, as seen in Figs.9a and 10b. The high MOSFET $\hat{I}_{O(max)}$ arises despite high power-loss because a 1000V, 150A switch rating is only achievable using five parallel connected 1000V, 28A modules which gives very low $R_{\theta JC}$ and $R_{\theta CH}$ values [Appendix-1]. coefficients extracted from data sheets

DEVICES	I_O 0.1Hz 20kHz (A)	I_O 50Hz 20kHz (A)	I_O 50Hz 5kHz (A)	P_Q (W)	η_{INV} (%)	Z (t_P)	Z (t_P,D)	$R_{\theta JC}$ K/W	$R_{\theta CH}$ K/W
DT47-MOSFET CASCODE	83	147	239	365 (57)	96	.159	.427	.063	.025
BSM191C MOSFET	85	131	148	683 (23)	93	.162	.429	.18/ 5	.05/5
BSM150GB-100D	34	65	127	179	97	.210	.461	.1	.038
MG150Q2YS1 HIGH SPEED	32	55	106	133	97	.191	.449	.156	.04
MG150Q2YS11 LOW SAT.	26	45	104	"	96	"	"	"	"
MG150N2YS1 1ST GEN.	20	36	75	"	95	"	"	"	"
MG150M2YK1 DARLINGTON	22	34	71	"	95	"	"	"	"

Table-1 Maximum usable current, $\hat{I}_O$, for $T_J = 110°C$, total average switch power-loss, P_Q, net inverter efficiency, η_{INV}, device thermal resistances and effective normalised impedances.

The higher $\hat{I}_{O(max)}$ of the IGBT, BSM150GB100D, [Fig.10a] over the high-speed IGBT, MG150Q2YS1, similarly, arises despite lower efficiency, illustrated in Fig.8, due to lower $R_{\theta JC}$. The increase in $\hat{I}_{O(max)}$ with f_O, seen in Fig.9, arises because of improved thermal filtering and shows that adaptive active-current-limiting would optimise device utilisation in VVVF applications, irrespective of device type.

Fig.9a gives usable $\hat{I}_{O(max)}$ assuming all switching loss is eliminated, and shows that for most devices a factor of three improvement appears possible at 20kHz. This is of interest because it gives an indication of the potential gain in device utilisation obtainable, in principle, using snubber networks or soft switching

The ordering of devices in Fig.9a is determined by on-state voltage and package thermal performance. The higher $\hat{I}_{O(max)}$ is obtained with the single stage BJT in the cascode configuration, the low-saturation-voltage IGBT has the higher $\hat{I}_{O(max)}$ of all IGBTs, and the MOSFET with its high $R_{DS(on)}$ has a relatively low $\hat{I}_{O(max)}$ compared with the faster IGBTs, despite good package thermal performance, because of its significantly higher on-state voltage.

If f_O is held constant at 50Hz and f_{SW} varied, maximum usable current $\hat{I}_{O(max)}$ varies for the devices varies as shown in Fig.10a. Corresponding η_{INV} graphs are given in Fig.10b. Fig.10a illustrates the penalty associated with high f_{SW} inverter operation because, except for MOSFETs, the fall off in usable $\hat{I}_{O(max)}$ is very rapid with increasing f_{SW}, even for the high-speed IGBT.

The main point of this section has been to show the variation of usable device current that is possible over a range of operating conditions in an application. Choice of device, and the optimum f_{SW} range over which it may be used, is facilitated by comparing $\hat{I}_{O(max)}$ and η_{INV} in the actual application, especially with varying load current. Despite the switch-mode operation of power-converters, the analysis is simplified when high carrier-frequency ratios are used because time-average effects are more easily approximated.

CONCLUSIONS

The data presented in Figs.8 to 10 and Table 1 is not meant primarily for device comparison, since some aspects of device performance are not well specified and variability exists in the way in which device performance is specified. The intention has been to demonstrate that usable device current varies with modulating signal frequency [Fig.9b], switching frequency [Fig.10], and the level of soft switching employed [c.f. Figs.9a and 9b]. Predicting usable current does not only require knowledge of device conduction and switching loss but also device thermal conditions, such as thermal impedance, equivalent power pulses for steady-state operation, and in the case of transient load changes thermal response to power waveform transients. With wide variation in power-electronics system input and/or output quantities and modulating and switching frequency possible [eg. VVVF inverters employing hysteresis current control] determining usable current in the presence of tolerance in device characteristics and operating conditions is a complex matter. Temperature-regulated active current limiting would considerably ease this by ensuring that power-stages are always usable up to their full capability under transient, as well as steady-state, conditions.

REFERENCES

1. P. L. Hower, "A comparison of bipolar and field-effect transistors as power switches", Proc. of IEEE Industry Applications Society Annual Meeting, 1980, pp.682-688.

2. P. L. Hower and J. B. Brewster, "A new method of characterizing the switching performance of power transistors", Proc. of IEEE Industry Applications Society Annual Meeting, 1978, pp.1044-1049.

3. G. Boker and K. Heumann, 'Comparison of IGBTs and HF-GTOs with respect to high-frequency inverter applications", Proc. of IEEE Power Electronics Specialists Conf., 1991, pp.551-556.

4. A. Petterteig and T. Rogne, "IGBT turn-off losses in hard switching and with a capacitive snubber", Proc. of European Conf. on Power Electronics and Applications, 1991, pp.203-208.

5. J. H. Rockot, "Losses in high-power bipolar transistors", IEEE Trans. on Power Electronics, Vol. PE-2, No.1, Jan. 1987, pp.72-80.

6. D. A. Grant and J. Gowar, "Power MOSFETs Theory and Applications", John Wiley & Sons Inc., London, 1989, pp.294-304.

7. V. Ikeda, J. Itsumi and H. Funato, "The power loss of the PWM voltage-fed inverter", Proc. of IEEE Power Electronics Specialists Conf., 1988, pp.277-83.

8. L. K. Mestha and P. D. Evans, "Analysis of on-state losses in PWM inverters", IEE Proc., Vol. 136, Pt. B, July 1989, pp.189-195.

9. J. W. Kolar, H. Ertl and F. C. Zach, "Calculation of the passive and active component stress of three phase PWM converter systems with high pulse rate", Proc. of European Conf. on Power Electronics and Applications, 1989, pp.1303-1311.

10. J. W. Kolar, H. Ertl and F. C. Zach, "Influence of the modulation method on the conduction and switching losses in a PWM converter system", Proc. of IEEE Industry Applications Society Annual Meeting, 1990, pp.502-510.

11. A. Boglietti, P. Ferraris and F. Profumo, "Losses evaluation in high-power devices PWM inverter motor drives", Proc. of European Conf. on Power Electronics and Applications, 1991, pp.386-392.

12. "GTR Module (IGBT) Data Book", Toshiba Corp., Japan, Pub. No.35060, 1990.

13. "Standard transistorized inverter", Toshiba Corp., Japan, TOSVERT-130G1 for driving general purpose AC motors, Publ. No. 87-05(A)QC64031B.

14. "GTR Module (IGBT) Application Notes", Toshiba Corp., Japan, Publ. No. 507D-A, 1991.

15. "GTR Module Data Book", Toshiba Corp., Japan, Publication No. 3504D,1989.

16. "Mitsubishi Power Module Data Book, Mitsubishi Electric Corp., Japan, Dec.1983.

17. "SIPMOS Semiconductors Data Book", Siemens AG., Munchen, Germany, 1990.

18. "Power Line Power Transistors", Marconi Electronic Devices, Lincoln, UK, Pub.No.P47, 1986.

19. V. Sasada and S. Matsubayashi, "New second generation IGBT", Proc. of Power Conversion and Intelligent Motion Conf., PCIM90, June 1990, pp.107-116.

20. J. Zubek, A. Abbondanti and C. J. Norby, "Pulse width modulated inverter motor drives with improved modulation", IEEE Trans. on Industry Applications, Vol. IA-11, No. 6, Nov./Dec. 1975.

21. P. D. T. Connor, "Practical Reliability Engineering", John Wiley & Sons Ltd., Chichester, 1985, pp.200-203.

22. US Military Handbook, "Electronic Reliability Handbook", MIL-HDBK-338, Vol. 1 of 11, 15 Oct. 1984, Section 7.0.

23. "Silicon Rectifier Data Manual", Motorola Inc., 1980, pp.21-2.21.

24. W. E. Newell, "Dissipation in Solid State devices - The magic of I^{1+N}, IEEE Trans. Industry Applications, Vol. IA-12, No. 4, 1979, pp.386-396.

25. "DT60T/DT62T - 75/90 Transistor Data Sheets", Westinghouse Electric Corp., Semiconductor Division, Youngswood, USA, 1982.

APPENDIX-1

SNGLE BJT	T_J (°C)	V_{QO} (V)	r_Q (mΩ)	K_{QMAX}	V_{DO} (V)	r_D (mΩ)	K_{DMAX}	W_{QSWoff} (mJ)	n	W_{QSWon} (mJ)	m
DT47 CASCODE	125	0.67	9.1	1.5	0.948	5.514	1.5	13.5	1	27.50	1.153
EMITTER MOSFET SMP60N06	"	0	20/3	1.150	--	--	--	--	--	--	--
		V_{BQO}	r_{BQ}	K_{BMAX}	β_{MIN}	--	--	--	--	--	--
BASE LOSS	"	0.76	4.27	1.362	4	--	--	--	--	--	--
MOSFET	T_J (°C)	V_{QO} (V)	r_Q (mΩ)	K_{QMAX}	V_{DO} (V)	r_D (mΩ)	K_{DMAX}	W_{QSWoff} (mJ)	n	Q_{RR} (μC)	di/dt (A/μs)
BSM191C	110	"	589 /5	1.114	0.583	3.825 /5	1.217	7.875	1	5x36.2	800
SERIES DIODE BR20035CT	125	--	--	--	0.317	3.038	1.0	--	--	--	--
IGBT	T_J (°C)	V_{QO} (V)	r_Q (mΩ)	K_{QMAX}	V_{DO} (V)	r_D (mΩ)	K_{DMAX}	W_{QSWoff} (mJ)	n	W_{QSWon} (mJ)	m
BSM150GB100D	125	1.565	14.35	1.125	0.948	5.514	1.0	16.00	0.527	23.38	1.153
MG150Q2YS1	"	1.324	8.338	1.333	0.948	5.514	"	23.05	1.122	27.50	1.153
MG150Q2YS11	"	0.864	8.484	1.227	0.948	5.514	"	47.62	1.147	27.50	1.153
MG150N2YS1	"	1.256	16.79	1.429	0.948	5.514	1.5	69.90	1.183	27.50	1.153
DARLINGTON MG150M2YK1	"	1.189	6.077	1.154	0.814	5.033	"	246.1	1.63	--	--

Table-2 Device conduction and switching loss coefficients extracted from data sheets